

REMARKS

Claims 1, 2 and 4 - 14 are pending in the present application, of which claims 5 and 11 have been withdrawn from consideration. By this Amendment, claims 1, 4, 6 – 10 and 12 have been amended. No new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated March 26, 2004.

Examiner Interview:

The courtesy extended by Examiner Vu to Applicant's representative during the June 17, 2004 personal interview is gratefully appreciated. The substance of such interview is incorporated in the following remarks.

Claim Objections:

Claims 4, 6 - 10 and 12 stand objected to due to the informalities set forth in item 2, pages 2 and 3 of the Action. However, it is respectfully submitted that each of claims 4, 6 - 10 and 12 has been amended to overcome their respective claim objections. Accordingly, withdrawal of such claim objections is respectfully requested.

As To The Merits:

As to the merits of this case, the Examiner relies on the newly cited reference of Tanaka (U.S. Patent No.: 6,100,589) in setting forth the following rejection:

claims 1, 2, 4, 6-10 and 12-14 stand rejected under 35 U.S.C. §102(b) as being anticipated by Tanaka. This rejection is respectfully traversed.

Independent claim 1, as amended, now calls for *a semiconductor substrate; a lower dielectric layer arranged on and in direct contact with the substrate and having an opening, a conductive portion filling the opening, and at least one dielectric member embedded in the conductive portion.*

With regard to these features, the Examiner asserts that Tanaka discloses “a semiconductor substrate (400); a lower dielectric layer (lower portion 160) arranged on the substrate and having an opening, a conductive portion (300) filling the opening, and at least one dielectric member (133a-133i) embedded in the conductive portion.”¹

However, the Examiner is mis-characterizing the teachings of Tanaka. More specifically, according to Tanaka, “the first electrode layer 300 is formed on an oxide film (insulating film) 410 which covers the surface of the semiconductor substrate.”²

Therefore, in Tanaka, the insulating film 410, and not the insulating interlayer (lower portion) 160, is arranged on and in direct contact the substrate 400. Moreover, the first electrode layer 300 is formed on the insulating film 410 and not in an opening of the insulating interlayer 160.

Further, it is respectfully submitted that during the June 17, 2004 personal interview, “Applicant’s representative pointed out that dielectric 160 is not arranged and in direct contact with the substrate. The Examiner agrees that Tanaka does not anticipate this feature.”³

¹ Please see, lines 1-4, page 4 of the Action.

² Please see, lines 29-31, column 6 of Tanaka.

Therefore, clearly Tanaka fails to disclose the features of claim 1 concerning *a semiconductor substrate; a lower dielectric layer arranged on and in direct contact with the substrate and having an opening, a conductive portion filling the opening, and at least one dielectric member embedded in the conductive portion.*

In addition, independent claim 1 also calls for *an interlayer dielectric film arranged on the lower dielectric layer and having a contact wiring; and an upper dielectric layer arranged on the interlayer dielectric film and having an upper opening, an upper conductive portion filling the upper opening, and at least one dielectric member embedded in the upper conductive portion, wherein the upper dielectric layer and the lower dielectric layer are electrically connected by the contact wiring.*

With regard to these features, the Examiner asserts that Tanaka discloses *an interlayer dielectric film (upper portion 160) arranged on the lower dielectric layer and having a contact wiring (120a-120c); an upper dielectric layer (lower portion 150) arranged on the interlayer dielectric film and having an upper opening, an upper conductive portion (200) filling the upper opening, and at least one dielectric member (130a-130i) embedded in the upper conductive portion, wherein the upper dielectric layer and the lower dielectric layer are electrically connected by the contact wiring.*

³ Please see, lines 2 – 4, page 3 of the Interview Summary Record dated June 17, 2004.

However, the Examiner's reliance on the insulating interlayer 160 of Tanaka for teaching both the lower dielectric layer and an interlayer dielectric film arranged on the lower dielectric layer is clearly unreasonable. Moreover, while Tanaka may disclose that the second insulating interlayer 150 is provided with a plurality of through holes, conductive members 110a to 110d, and not the second electrode layer 200, are embedded into the through holes provided in the insulating interlayer 150.

In other words, Tanaka fails to disclose the additional features of claim 1 concerning *an interlayer dielectric film arranged on the lower dielectric layer and having a contact wiring; and an upper dielectric layer arranged on the interlayer dielectric film and having an upper opening, an upper conductive portion filling the upper opening, and at least one dielectric member embedded in the upper conductive portion, wherein the upper dielectric layer and the lower dielectric layer are electrically connected by the contact wiring.*

Furthermore, independent claims 6 and 12 are drawn to similar embodiments of independent claim 1 and therefore define over Tanaka for similar reasons as delineated above.

In view of the aforementioned amendments and accompanying remarks, Applicant submits that the claims, as herein amended, are in condition for allowance. Applicant requests such action at an early date.

Response under 37 C.F.R. §1.111

Attorney Docket No.: **021067**

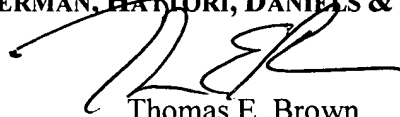
Serial No.: **10/076,355**

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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